SE | ETRX | III CBGS

DCD. 28|5|14

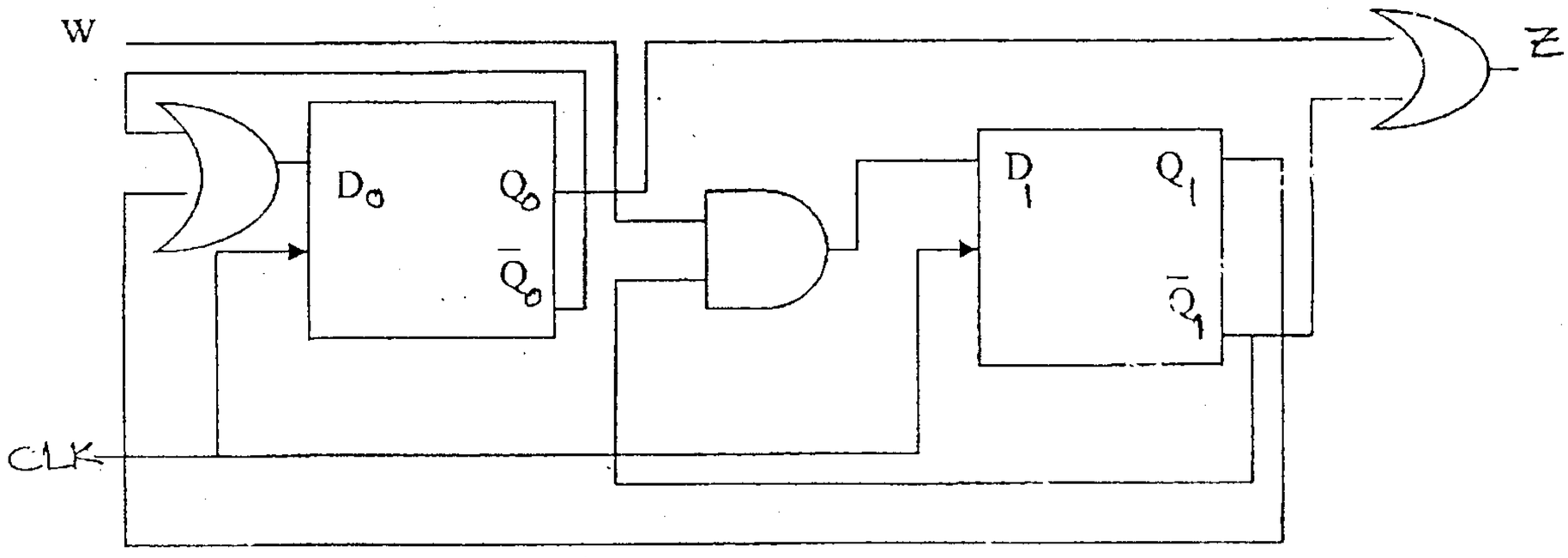
QP Code : NP-18678

(3 Hours) **[Total Marks : 80**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Solve any **three** from remaining **5** questions.
(3) Draw **neat** diagrams wherever **necessary**.

1. **(A)** Implement the following function using NOR gates only (after reduction using K map) **10**
F = π M (1,2,4,7,11,13) . d (9,15)
(B) Design a MOD 6 asynchronous counter and explain glitch problem. **10**

2. **(A)** Analyze the clocked synchronous machine given below. Write excitation equations, excitation/transition table and state /output table (Use state names A - D for Q1-Q2=00–11). Also draw the state diagram. **10**



(B) Design a 1 digit BCD adder using IC 7483 and explain the operation for **$(0111)_{BCD} + (1001)_{BCD}$**. **10**

3. **(A)** Write a VHDL code for 8:1 Multiplexer with active low enable input. **10**

(B) Design a mealy sequence detector to detect a sequence ----1101----using D flip-flops and logic gates. **10**

4. **(A)** Design a circuit with optimum utilization of PLA to implement the following functions **10**
$F1 = \sum m (1, 2, 3, 6, 9, 11)$
$F2 = \sum m (0, 1, 6, 8, 9)$
$F3 = \sum m (2, 3, 8, 9, 11)$

(B) Implement following function using 4:1 line MUX and NAND gates. **10**
$F (A, B, C, D) = \sum m (1, 2, 6, 7, 10, 12, 13)$

5. **(A)** Design a 8 bit binary up counter using MSI counter IC 74163, draw a circuit diagram and explain working. **10**

(B) Eliminate redundant states and draw reduced state diagram. **10**

PS	NS		O/P
	X = 0	X = 1	Y
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

6. Write short notes on (Any THREE): **20**
1. XC 4000 FPGA Architecture
2. Stuck at '0' and stuck at '1' fault
3. Master Slave JK flip flop
4. 2 input TTL NAND gate

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Con. 11974-14.